Hardware report Alex and Ding

This section details the hardware team’s work since the first report. It has been broken down into two main sections: the input stage and the output stage. Each section details the relevant circuits along with any problems encountered by the team. In the first report we said that we would continue to look at signal generation in hardware, this has not been the case as our software team have been capable of producing signals which meet the specifications set. The only signal they haven’t created is a triangle wave, which has instead been realised by running the square wave output through an integrator circuit.

**Input stage:**

The input stage could be divided into three parts, Comparator, Potential Divider and Frequency Divider. They are designed to transfer analogue waveforms into digital binary signal so that the software team would be able to detect the frequency of the input signals by their board. Meanwhile the hardware team must guarantee the voltage of input signals are lower than 3V in order to protect their PCB board. The following sections will individually introduce each ‘part’, detailing the design, theory, purpose and limitations, before a short section introduces how they are combined.

**Comparator:**

|  |  |  |  |
| --- | --- | --- | --- |
| Component used in the final circuit | Number of components | Value | Components be replaced |
| LM311 | 1 | N/A | LM393 |
| Resistor | 1 | 3.3kΩ |  |

A comparator circuit would be able to transfer square, triangle and sine wave into a square wave digital signal as output. It is designed to produce well limited output voltages that easily interface with digital logics.

As our team decided to implement a mixed digital approach, the Appendix includes the circuit diagram of comparator. Initially we used ½ of LM393 circuit (shown in the lecture) but found the output to be particularly noisy and the up frequency limit was quite low. As an alternative, we tried comparator with Hysteresis, with the intention of improving the noise performance, however the results of testing showed it made things worse than before. In order to improve the performance, we designed a circuit as figure 2 shows. LM393 is replaced by LM311, with two 100nF decoupling capacitors are added at VEE and VCC to reduce the noise effect. A 3MΩ potential meter is used to vary the output voltage in order to make it fit with other circuits’ requirements.

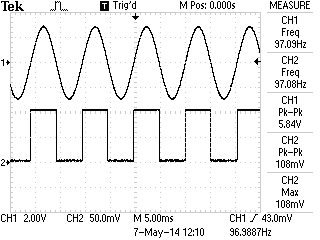


Figure 2. Output of Comparator

Figure 2 is the oscilloscope’s screenshot of our comparator’s output. Channel 1 is a 5.84V sine wave input in 97.1Hz. Channel 2 is the output of comparator circuit. As the figure shows, frequencies of two signals are almost the same, which proved that comparator was working as per expectations.

Limitations:

* Amplitude: Power supply: +/- 15V Input voltage: Maximum of twice as power supply

According to the datasheets [1] power consumption of LM 311 is +/- 15V. If the power supply to it is lower than that level, the circuit still could work as expected but we found that when the voltage of the input signal was larger than the twice of comparator’s working voltage an extra period of square wave appeared at the output of comparator. Figure 3 shows that effect. Comparator got working voltage around 4V at that time when voltage of input signal is higher than 8.1V comparator didn’t operate as before.

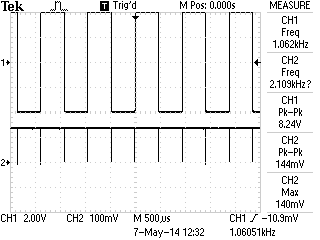
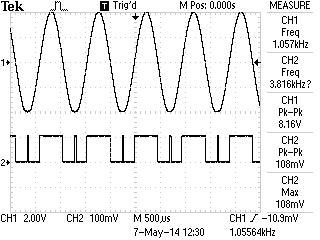


Figure 3. Extra period effect

* Frequency: Maximum: 8MHz

According to the slew rate effect (figure 4) of circuit when the frequency of input increase to a high range, the voltage of output signal will start to decrease. In our design comparator is followed by a frequency divider circuit, that circuit has a minimum voltage requirement about input signal which should be higher than 1.4V, otherwise counters would ignore that signal.

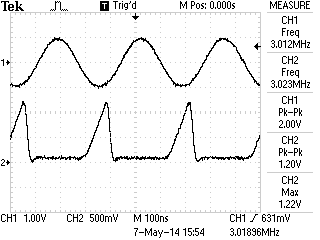


Figure 4. Slew rate effecting comparator’s output

In this case we connected the output of comparator to the input of frequency divider during testing, to find the maximum significant frequency that comparator can produce. Figure 4 is the maximum frequency.



Figure 5. Highest significant frequency comparator can achieve

Channel 1 is the output of a decay counter Channel 2 is the output of comparator. Comparator’s working voltage at that time was 14.3V. Signal input to comparator is a 1.08V sine wave. The image shows Channel 2’s frequency as 10 times larger than Channel 1’s, meaning the frequency divider could still detect the comparator’s output.

**Frequency divider:**

|  |  |  |  |
| --- | --- | --- | --- |
| Component used in the final circuit | Number of components | Value | Components be replaced |
| 74LS90N | 3 | N/A |  |

In order to help the software team to measure high frequency waves, we designed a frequency divider circuit as shown in the Appendix. All of 74LS90N are connected in the way of decay counter. In this case connecting 3 counter circuits in series gives us a frequency divider which could divide input digital signal by 1000. Figure 5 shows how one 74LS90N works as a decay counter. Channel 2 is the TTL digital signal input and Channel 1 is the output. Measurement at right side of the diagram proves that dividing function is working as anticipated.

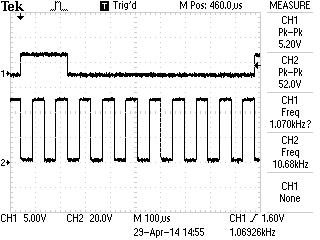


Figure 6. Frequency divider ÷ 10

Limitation:

* Amplitude:

According to the datasheet of 74LS90N, both the power supply and the input signal voltage must be equal or lower than 7V. [2] This is the reasoning behind placing a potential meter at the output of the comparator, in order to protect the frequency divider.

* Frequency:

In the datasheet the ideal highest counting frequency of 74LS90N is 42MHz. Due to our circuit design, the frequency divider only receives input from the comparator’s output. In this case the highest frequency that the divider circuit can produce is enslaved to the comparator’s output. The maximum frequency we recorded in that situation is shown in Figure 4.

Problem:

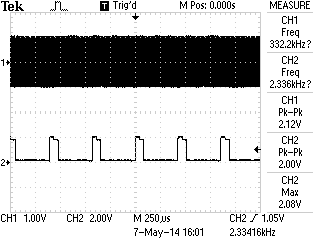


Figure 7. Frequency divider ÷ 1000

Figure 7 shows the performance of when 3 decay counters were connected together. The input frequency (CH1) from comparator is 2.3MHz, for some reason that scope can’t measure it in that scale. CH2 is the output of frequency divider, measurement of ch2’s frequency proves that counters are working as expected. Problematically, the outputs of the divider are not in a perfect square wave form. There is a slight step at the peak of square wave. Whilst being unsure of what caused this, it didn’t affect our result of frequency measurement.

**Potential divider:**

|  |  |  |  |
| --- | --- | --- | --- |
| Component used in the final circuit | Number of components | Value | Components be replaced |
| Potential meter | 1 | 3MΩ |  |
| Potential meter | 1 | 2MΩ |  |

The main aim of using potential divider circuits is to reduce the voltage of each circuit output and protects the circuit following it.

3MΩ potential meter is placed in comparator circuit to make sure that the output of it is always lower than 7V. 2MΩ potential meter is placed at the output of frequency divider to protect software team’s board which only could take 3.3V input signal as maximum.

**Output stage**

The output stage consists of three circuits: an integrator, an amplifier and a DC offset. This stage has been designed to transform the low level signals output from the board to a useable level. Each of the three sub-circuits was first built and tested separately before being integrated into the master circuit. All of the op-amps used in each circuit have de-coupling capacitors at the power inlet for the IC to maintain a smooth supply voltage and reduce noise interference. The following section details the work carried out to create each individual circuit. This is followed by a short section describing the integration of each sub-circuit into the overall output stage circuit. See the appendix for all circuit diagrams.

**Integrator**

The first circuit in the output stage is an integrator. While its operation may seem obvious from its name, it is one of the more subtle properties for which we have chosen to use this circuit; when a square wave is input into the integrator the output will be a triangle wave. We required this circuit as the software team found they were unable to generate triangle waves at the frequencies required by the specifications laid out, and we found that the hardware solutions also failed to operate at the required frequency (see the previous report for details of this). With the software team able to generate very high frequency square waves this solution seemed most appropriate as the only immediately obvious limitation is the slew rate of the op-amp used. This circuit’s output is controlled by the capacitor charging and discharging which, with a square wave input, forms the triangle wave output desired. For the initial prototype of the circuit we used a 741 op-amp and a 1µF capacitor; however during testing we realised that the RC time constant became a limiting factor for the frequency range over which the integrator could operate and provide a clean triangle wave output. We decided that switching the capacitor would be the best solution for this and found that a 100pF capacitor allowed operation up to the highest frequency range while a 2.2µF capacitor was required to get a good triangle wave at 1Hz. Table 1, below, shows the useable frequency range for a selection of capacitors.

|  |  |
| --- | --- |
| **Capacitor** | **Frequency Range** |
| 100pF | 30kHz – 3MHz |
| 15nF | 350Hz - 220kHz |
| 1µF | 10Hz - 1kHz |
| 2.2µF | 0.2Hz – 20Hz |
| 47µF | 0.2Hz – 1Hz |
| *Table 1: Operational frequency range of various capacitors* | |

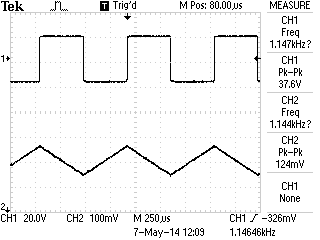
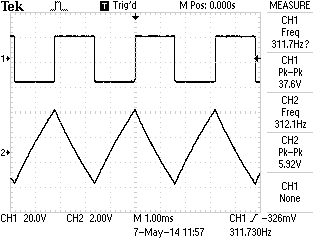


Figure 8 The integrator with a 47nF capacitor on the left and on the right the integrator with a 68uF capacitor

These results show that no single capacitor is able to operate of the entire range of frequencies desired. Larger capacitors are required for lower frequencies to ensure that the signal doesn’t saturate, while smaller capacitors are needed with increasing frequency due to the voltage drop encountered. To achieve the full range of frequencies laid out in the specification different capacitors are required to be switched into the circuit, with the user selecting the appropriate capacitor for the desired frequency range. The circuit diagram in the appendix shows how, by using a 1 to 4 switch, this functionality is achieved.

There were two major limitations to the operation of this circuit. The first was the slew rate of the LM741 op-amp (0.5V/µs [3]); it was unable to handle the highest frequencies. We changed it out for a LM318 op-amp which overcame this problem due to its higher slew rate of 50V/µs [4]. The second major limitation is the fact that as the frequency approaches the upper limit for the capacitor being used there is a significant voltage drop. Fortunately there is a large overlap between each capacitor’s operating ranges which counters this problem, except at the highest frequencies where there is no overlap. This proved particularly problematic as the output from the board was already a very low level signal. Our solution was to run the output from the board through a gain stage first, followed by the integrator then running it through a final gain stage.

**Amplifier**

The amplification is carried out using a relatively standard set up for a non-inverting operational amplifier. The output from the board is limited to a maximum level of 3.3V, hence the need for the amplifier circuit. To allow for the gain to be adjusted the pair of resistors, that form a potential divider in the feedback loop, have been replaced with a 200kΩ potentiometer and a 10kΩ resistor to ground. Adjusting this pot changes the gain of the amplifier. Table 2 shows the frequency response of the amplifier with a fixed gain of 2.

|  |  |  |
| --- | --- | --- |
| **Frequency** | **Vin** | **Vout (Gain = 2)** |
| 0.2Hz | 2.00 | 4.00 |
| 1Hz | 2.00 | 4.00 |
| 10Hz | 2.00 | 4.00 |
| 100Hz | 2.00 | 4.00 |
| 1kHz | 2.00 | 4.00 |
| 10kHz | 2.00 | 4.00 |
| 100kHz | 2.00 | 4.00\* |
| 1MHz | 2.00 | 2.00\* |
| 10MHz | 2.00 | 0.28\* |
| *Table 2: Frequency response of the amplifier* | | |

\*At these frequencies the slew rate of the op-amp became a limiting factor.

As can be seen up to 100kHz the amplifier worked as expected however beyond this there were several problems. Figure 2 shows the scope capture of the circuits output.

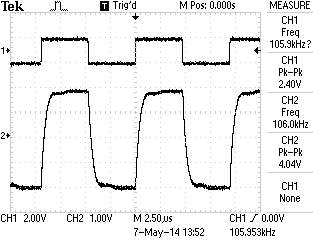


Figure 9 Scope capture from the amplifier at 100kHz

Theoretically the LM318 should be able to handle a signal of about 2MHz for a 4V output.

Where:

* f is the frequency in Hz
* SR is the slew rate per second
* V is the peak to peak voltage of the output

It is therefore surprising to see that the output signal is showing signs of distortion that can be caused by having too low a slew rate. Inputting higher frequencies the distortion became worse.

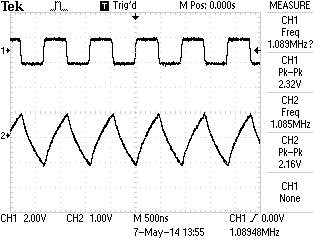


Figure 10 Op-amp fed with a 1MHz signal

We tried adjusting the gain of the amplifier circuit, which improved the shape of the output signal, see figure 4.

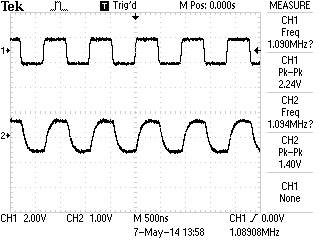


Figure 11 The result of changing the amplifiers gain

Unfortunately we have been unable to work out what is causing this problem.

**DC offset**

The DC-offset circuit’s operation is fairly simple, taking the input signal and adding a constant DC voltage to it, allowing the user to shift the signal to the required operating level. This circuit also makes use of a LM318 op-amp with negative feedback. The offset voltage input is taken from the power supply and then run through a potentiometer to set its level. Our circuit combines an averager and an amplifier. First the input signal and the DC-offset signal are averaged, then amplified. When the gain of the op-amp is set to two the output is that of a true adder circuit.

|  |  |  |
| --- | --- | --- |
| **Frequency** | **Vin** | **Vout (Gain = 2)** |
| 0.1Hz | 4.00 | 8.00 |
| 1Hz | 4.00 | 8.00 |
| 10Hz | 4.00 | 8.00 |
| 100Hz | 4.00 | 8.00 |
| 1kHz | 4.00 | 8.00 |
| 10kHz | 4.00 | 8.00 |
| 100kHz | 4.00 | \* |
| 1MHz | 4.00 | \* |
| 10MHz | 4.00 | \* |
| *Table 3: Frequency response of the DC offset circuit* | | |

\*Function generator possibly causing problems (instek GFG-8210)

One of the limiting factors for the DC-offset is that it’s upper and lower limits are set by the supply voltage to the op-amp; if it reaches this point the signal saturates and becomes a constant DC level. We also encountered similar problems with this circuit to those that we had already seen in the amplifier circuit; this time, however, the input signal from the function generator also became distorted.

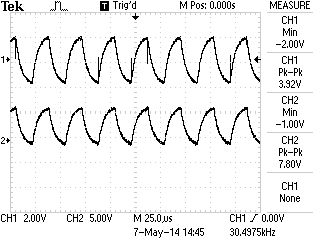


Figure 12 DC-offset output showing distortion

**Combining the circuits**

When it came to combining the circuits we realised that we could use our DC-offset circuit as an amplifier as well by replacing one of the feedback resistors with a potentiometer. We decided to keep the amplifier we had already created and use it to feed the integrator circuit, with the DC-offset/amplifier circuit being placed last in the chain. A simple bypass, consisting of a toggle switch, allows for the user to select whether the output from the board is run through the integrator stage or not. We encountered an increased noise level when the signal passed through both op-amps.

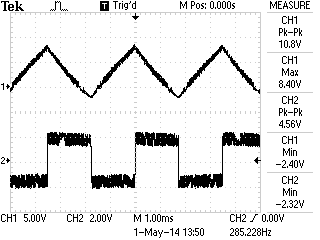


Figure 13 The output signal became very noisy in the final circuit

**Improvements**

There are a few issues with individual circuits which have already been discussed that would need to be solved before the function generator and frequency meter reach their final implementation stage; in addition to this there are a couple of other points for improvement of the overall package. With more time we would like to have been able to provide software control over all of the adjustable components (switches and potentiometers). To do this would require that all of the components be replaced with their digital counter-parts and for the software team to provide the relevant control signals. We would also have liked to create our own power supply, similar to the lab supply, which would have outputs for +/- 15V, 5V DC and 10V DC.

# References

|  |  |
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| [1] | Instruments, TEXAS, "LM111-N/LM211-N/LM311-N Voltage Comparator," March 2013. [Online]. Available: http://www.ti.com.cn/general/cn/docs/lit/getliterature.tsp?genericPartNumber=lm311-n&fileType=pdf. [Accessed 8 May 2014]. |
| [2] | National Semiconductor, June 1989. [Online]. Available: www.datasheetarchive.com/74LS90N-datasheet.html. [Accessed 08 May 2014]. |
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| [4] | Texas Instruments, "LM318 Datasheet," March 2013. [Online]. Available: http://www.ti.com.cn/cn/lit/ds/symlink/lm118-n.pdf. [Accessed 7 May 2014]. |

# Appendix

